Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Currently Amended) A method for identifying tri-state logic connected to a selected node of an integrated circuit by evaluating a netlist at the node comprising the steps of:

selecting a circuit configuration to be identified, wherein the circuit configuration defines a tri-state logic configuration;

identifying [any of said] known circuit configurations at the node; [and]

identifying [any] probable circuit configurations at the node; and

determining whether the selected circuit configuration is an identified known or identified probably circuit configuration.

2. (Original) The method as defined in claim 1, wherein the step of selecting a circuit configuration includes identifying a complementary pass FET circuit configuration.

3. (Original) The method as defined in claim 1, wherein the step of selecting a circuit configuration includes identifying a special complementary pass FET circuit configuration.

4. (Original) The method as defined in claim 1, wherein the step of selecting a circuit configuration includes identifying a gate output circuit configuration.

5. (Original) The method as defined in claim 1, wherein the step of selecting a circuit configuration includes identifying a RAM cell circuit configuration.

6. (Original) The method as defined in claim 1, wherein the step of selecting a circuit configuration includes identifying a feedback FET circuit configuration.

7. (Original) The method as defined in claim 1, wherein the step of selecting a circuit configuration includes identifying a single pass FET circuit configuration.

8. (Currently Amended) A system for identifying tri-state logic connected to a selected node of an integrated circuit by evaluating a netlist at the node comprising:

means for selecting a circuit configuration to be identified, wherein the circuit configuration defines a tri-state logic configuration;

means for identifying [any of said] known circuit configurations at the node; [and]

means for identifying [any] probable circuit configurations at the node; and

means for determining whether the selected circuit configuration is an identified known or identified probably circuit configuration.

9. (Original) The system of claim 8, further comprising:

means for identifying tri-state logic connected to a selected node of an integrated circuit by evaluating a netlist at the node comprising:

means for selecting complementary pass FET circuit configurations.

10. (Original) The system of claim 8, further comprising:

means for identifying tri-state logic connected to a selected node of an integrated circuit by evaluating a netlist at the node comprising:

means for selecting special complementary pass FET circuit configurations.

11. (Original) The system of claim 8, further comprising:

means for identifying tri-state logic connected to a selected node of an integrated circuit by evaluating a netlist at the node comprising:

means for selecting gate output circuit configurations.

12. (Original) The system of claim 8, further comprising:

means for identifying tri-state logic connected to a selected node of an integrated circuit by evaluating a netlist at the node comprising:

means for selecting RAM cell circuit configurations.

13. (Original) The system of claim 8, further comprising:

means for identifying tri-state logic connected to a selected node of an integrated circuit by evaluating a netlist at the node comprising:

means for selecting feedback FET circuit configurations.

14. (Original) The system of claim 8, further comprising:

means for identifying tri-state logic connected to a selected node of an integrated circuit by evaluating a netlist at the node comprising:

means for selecting single pass FET circuit configurations.

15. (Currently Amended) A computer readable storage medium containing program code for identifying tri-state logic connected to a selected node of an integrated circuit and marking each such identified FET by setting a flag in a data structure associated with the FET comprising:

a first code segment configured to select a circuit configuration to be identified, wherein the circuit configuration defines a tri-state logic configuration;

a second code segment configured to identify [any of said] known circuit configurations in a netlist; [and]

a third code segment configured to identify probable circuit configurations at the node in a netlist; and

a fourth code segment configured to determine whether the selected circuit configuration is an identified known or identified probably circuit configuration.

16. (Original) The program code of claim 15, wherein said second code segment is further configured to set a complementary pass FET flag in the data structure for the identified elements that comprise a complementary pass FET.

17. (Original) The program code of claim 15, wherein said second code segment is further configured to set a special complementary pass FET flag in the data structure for identified elements that comprise a special complementary pass FET.

18. (Original) The program code of claim 15, wherein said second code segment is further configured to set a gate output flag in the data structure for the identified elements that comprise a gate output.

19. (Original) The program code of claim 15, wherein said second code segment is further configured to set a RAM cell flag in the data structure for the identified elements that comprise a RAM cell.

20. (Original) The program code of claim 15, wherein said second code segment is further configured to set a feedback FET flag in the data structure for the identified elements that comprise a feedback FET.

21. (Original) The program code of claim 15, wherein said second code segment is further configured to set a single pass FET flag in the data structure for identified elements that comprise a single pass FET.